Claims

1. Method of generating instruction words to trigger functional units in a processor, where in a configuration phase, a sequence of primary instruction words deriving from a translation of a program code is produced, each primary instruction word consisting of several instruction word parts and each instruction word part being intended to trigger a functional unit, and the instruction word parts in one or several primary instruction words serving to perform a data-stationary command, and each primary instruction word undergoing a fractionation into smaller word parts and, in an execution phase, a synthesis of a secondary instruction word corresponding to a primary instruction word is performed out of the smaller word parts, characterized in that each of the instruction word parts (4) serving to execute the data-stationary command being assembled as complex words (17) in a complex word sequence (18) and in a row of a complex word table (5) indicated by a complex word pointer (6), in that upon synthesis of secondary instruction words (15) that is to contain a sequence of instruction word parts (4) pertaining to the execution of the data-stationary command in an execution memory (9) the occurring associated complex word pointer (6) is recognized, in that in the row indicated by the complex word pointer (6) in the complex word table (5), the complex word sequence there deposited (18) is read out, in that the complex words (17) contained in it are stored parallelwise in dependence on the current secondary word in the corresponding

row and column of the secondary instruction word memory (7) by the several assignments internal to the complex words, in that corresponding to an elective secondary instruction word memory sequence (16) firstly the current secondary instruction word (15) arrives by way of an instruction word output (11) at the corresponding functional unit (12) of the processor (13) for processing, and secondly, it is processed in a secondary instruction word production (10) which at its output places in readiness an additional secondary instruction word (15) to be stored in the secondary instruction word memory (7).

2. Method according to claim 1, characterized in that a fixedly programmed secondary instruction word memory sequence (16) is established.

3. Apparatus for generating instruction words to trigger functional units in a processor having functional units, having an instruction word memory associated with said functional units, and having an instruction word memory for storage of instruction words already generated, having a latitude at least equal to the bit latitude of the secondary instruction word, the instruction word buffer consisting of a memory with elective or fixedly programmed row access, characterized in that the secondary instruction word memory (7) is associated with a read-only or write-and-read complex word table (5) in the form of a matrix register file.